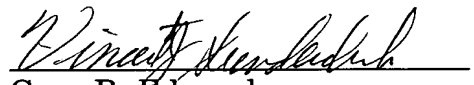
REMARKS

Entry of the amendments to the specification, claims and abstract before examination of the application is respectfully requested. These claims patentably define over the art of record.

If there are any questions regarding this Preliminary Amendment or the application in general, a telephone call to the undersigned would be appreciated since this should expedite the prosecution of the application for all concerned.

If necessary to effect a timely response, this paper should be considered as a petition for an Extension of Time sufficient to effect a timely response, and please charge any deficiency in fees or credit any overpayments to Deposit Account No. 05-1323 (Docket # 095309.56351US).

Respectfully submitted,



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Automatic addressing on bus systems

Background and Summary of the Invention

[0001] This application claims the priority of German patent document 102 61 174.2, filed December 20, 2002 (PCT International Application No. PCT/EP2003/012986, filed November 20, 2003), the disclosure of which is expressly incorporated by reference herein.

[0002] The present invention is directed ~~relates~~ to a method and apparatus for automatic address allocation by control ~~appliances~~ devices connected to a bus system in a ~~means of transport~~ vehicle, where the control ~~appliances~~ devices interchange data using transmission/reception units via a common data bus line, and the control ~~appliances~~ devices simultaneously access the data sent using the common data bus line. ~~The invention also relates to a bus system for carrying out the method.~~

[0003] In order to allow communication between control ~~appliances~~ devices in data bus systems, [[these]] the control ~~appliances need to~~ devices must have an individual address, which ~~. This respective individual address~~ allows the control ~~appliances~~ devices (or [[the]] "subscribers") in the data bus system to interchange messages and data with one another. In particular, it is possible to send messages directly to any subscribers in the data bus system, and it [[. It]] is normally also possible to ascertain the sender of a message.

[0004] In ~~the case of~~ address setting or allocation, it is necessary to ensure that the correct addresses are allocated to the appropriate subscribers. In particular, in order to avoid interference, the [[The]] same addresses must not be allocated ~~a plurality of~~ multiple times to different subscribers~~, in order to avoid interference~~. It should be a simple matter to handle the incorporation of a further subscriber into the data bus system and the associated address expansion.

[0005] "Daisy Chain" connections are frequently used in data bus systems on ~~means of transport~~ vehicle in order to configure the control ~~appliances~~ devices connected to the data bus system, particularly in order to make address settings.

[0006] A "daisy chain" connection is an individual ~~data line in the form of a~~ point-to-point data line connection which is ~~in the form of~~ a series or ring connection between a central control unit [[,]] (~~"~~the "master"~~)~~ [[,]] and the other subscribers[[,]] ~~"~~(the "slaves"~~)~~, in the "daisy chain" connection. [[The]] In a "daisy chain" connection, ~~is distinguished in that~~ a signal emitted by the central processing unit on the data line reaches only the first subscriber, is forwarded therefrom to the next subscriber, which in turn forwards the signal to the next subscriber etc. All subscribers can receive identical signals ~~by virtue of~~ when the signals are not [[being]] altered upon forwarding. In addition, in contrast to other bus systems, any subscriber in the chain can change one or more signals before it forwards the signal. The time-delayed forwarding allows a plurality of messages to be forwarded on the "daisy chain" connection, for example the second

subscriber can forward an electrical signal to the third subscriber while the master is already sending the next signal to the first subscriber.

[0007] In [[the]] a "daisy chain" connection, the signal return path generally runs directly from the last slave in the chain to the master. Unidirectional communication is permitted on the signal return path. Alternatively, the signal return path may be terminated at the last subscriber by means of a resistor, in which case the data lines should then be in bidirectional form.

[0008] Subscribers in a "daisy chain" connection have at least two interfaces for data interchange or for communication via the bus system. One of the two interfaces~~, particularly~~ (in particular, the first interface) [[,]] is in the form of a communication interface for receiving data from a subscriber which is connected upstream in the "daisy chain" connection, while the ~~. A subscriber's~~ second interface is ~~provided as~~ a communication interface for connection to a downstream subscriber in the bus system. If the "daisy chain" connection is bidirectional, the communication interfaces likewise need to be of bidirectional orientation.

[0009] A bus system which is designed using a "daisy chain" connection can only provide communication from master to slave or ~~from slave to master~~ vice versa. There is no provision for actual communication between the slaves [[,]] (that is, [[to say]] the subscribers in the bus system).

[0010] The fact that in a "daisy chain" connection the signals are forwarded from subscriber to subscriber in sections means that the "daisy chain" connection

is often called a "non-jointly used connection". In contrast ~~to this~~, "jointly used connections" are those which can be accessed by the subscribers with equal authority and where all subscribers can receive data simultaneously on account of the electrical or optical connection to the data line, as is implemented in the Control Area Network (CAN) protocol, for example.

[0011] Often, the address configuration for the subscribers in an arbitrary bus system is obtained using a (sub)bus system, which is constructed from a "daisy chain" connection[[,]] (that is, [[to say]] a non-jointly used connection). ~~The data~~ Data communication between the subscribers in the data bus system takes place using an additional, jointly used connection which allows individual communication with equal authorization on account of the actual data protocol between the subscribers.

[0012] German patent document DE 100 38 783 discloses a method and an apparatus for automatic address allocation to a plurality of subscribers in a bus system using "daisy chain" connection. Upon ~~receiving~~ receipt by the first interface of an unmistakable, explicit command from the master in a data packet for address allocation ~~which is received on the first communication interface~~, each slave subscriber stores the part which is to be interpreted as an address in an address memory which can be accessed by the respective subscriber, and forwards the data packet with the same command and an altered address value to a neighboring subscriber via the second interface.

[0013] German patent document DE 37 36 081 A1 discloses a method and an apparatus for address setting by subscribers which are ~~connected to a bus. The~~

~~subscribers are~~ connected to a central processing unit via a bus. In addition, the subscribers on the bus are connected in series by means of a "daisy chain" connection coming from the central processing unit. The subscribers' address setting is obtained using the "daisy chain" connection. A signal with a particular binary value on the "daisy chain" connection at the input of the first subscriber causes the latter to pick up an available address on the bus from a data packet produced in the central processing unit and to output the particular binary value to the "daisy chain" connection. The subscriber sends the address picked up to the central processing unit as a response. The method then continues at the neighboring subscriber.

[0014] ~~US-A-5 583 754~~ U.S. Patent No. 5,583,754 and French patent document FR-A-2 214 385 each describe a data bus system of the generic type, with a central control ~~applicance~~ device and periphery components.

[0015] German patent document DE196 21 272 A1 discloses an addressing apparatus for a slave station in a serial bus system and a method for addressing a slave station. The slave stations containa switching apparatus which is coupled into the data line to the downstream slave station in order to interrupt the data line on the basis of a switching signal from the control device.

[0016] ~~It is now the~~ One object of the present invention is to provide a method and a bus system which optimizes [[the]] automatic address allocation in a bus system with a common data line.

[0017] This and other objects and advantages are achieved by the method and apparatus according to the invention, in which an ~~The invention achieves this object by means of the features of claim 1. To this end, a period of~~ address allocation period is started by means of a message on the jointly used data bus line. ~~After that, the message is taken as a basis, in~~ During the address period ~~of address~~ allocation, the message is taken as a basis for electrically breaking the common data bus line into individual subsections by virtue of the control ~~appliances~~ device which are to be addressed using a respective isolating means ~~for the purpose of electrically breaking the common data bus line~~. In addition, the control ~~appliances~~ devices which are to be addressed place their respective transmission unit at a transmission potential.

[0018] Depending on the bus system chosen, the [[term]] data bus line ~~covers~~ may be in the form of single-wire, [[or]] two-wire or multiwire data lines.

[0019] References herein to the [[The]] "simultaneous" reception of data sent on the data bus by means of the control ~~appliances~~ devices does not mean absolutely simultaneous reception, but rather reception in a time interval which covers the propagation of the electromagnetic wave on the data bus line.

[0020] One advantage of this arrangement is that a common data bus line is split into individual subsections [[for]] during the period of address allocation, ~~which means~~ so that a "daisy chain" connection[[,]] (particularly a "non-jointly used" connection), topology is obtained between the control ~~appliances~~ devices which are to be addressed as bus subscribers.

[0021] Since the common data bus line is used for addressing, no additional data bus line is required between the control ~~appliances~~ devices. In addition, the control ~~appliances do~~ devices need not need [[to]] be equipped with a further bus protocol, such as would be necessary in order to be able to communicate via [[the]] such an additional data bus line for addressing. Standard control ~~appliances~~ devices, in which the address setting is intended to be performed using the inventive method, therefore need [[to]] be altered only to a minimal extent.

[0022] The method has the particular advantage that it can also be used for bus systems containing subscribers with equal authorization[[,]] (that is, [[to say]] not a master/slave system as described above). The address allocation merely needs to be initiated by a control ~~appliance~~ device using a signal.

[0023] The method according to the invention also has the advantage that, in contrast to known addressing methods, the master can be ~~positioned~~ located at any position in the bus system, rather than ~~. The master thus does not need to be positioned~~ at the start or end of the data bus line, as is ~~the case~~ required with a "daisy chain" connection. The reason for this is that the start signal for address allocation is obtained at a time at which the common connection is available to all control ~~appliances~~ devices.

[0024] Since the master can be positioned in the bus system as desired, it is a simple matter to extend the address allocation to other control ~~appliances~~ devices in the existing bus system. ~~By way of~~ For example, when control ~~appliances~~ devices are arranged in series and there is a master at an arbitrary

position, the control ~~appliances~~ devices can be incorporated into the address allocation to the right and/or left of the master.

[0025] A further advantage is that the method ~~for address setting~~ according to the invention can be used in bus systems in which ~~not~~ less than all control ~~appliances~~ devices in the bus system are involved in the addressing method. (That is, ~~that is to say, by way of~~ for example, control ~~appliances~~ devices configured in standard fashion already exist on the bus system). This is ensured, in particular, by virtue of just control ~~appliances~~ devices which are to be addressed being involved in the method.

[0026] The method can ~~likewise~~ also be applied when a further control ~~appliance~~ device (which is to be addressed) is added to or removed from the bus system, since all control ~~appliances~~ devices to be addressed are involved in the address allocation.

[0027] The method is not limited [[just]] to bus systems connected in series. Rather, it may also be used on bus systems with a ring structure, in particular.

[0028] It is advantageous for the transmission unit in the control ~~appliance~~ device which is to be addressed to turn on and send a signal, because this ensures that there is an electrical parameter for determining whether there is a further control ~~appliance~~ device which is to be addressed on the data bus line.

[0029] The address to be allocated is independent of the position of the subscriber in the bus system, since the check to determine whether there is a further downstream control ~~appliance~~ device to be addressed takes place after a

time T_{SG} which is individually stipulated for each control ~~appliance~~ device which is to be addressed. This means that the address to be allocated is likewise transmitted to the control ~~appliance~~ device independently of the position of the control ~~appliance~~ device. There is thus no address allocation required, such as rising address, in line with the order of the position of the control ~~appliances~~ devices in the bus system.

[0030] One advantage of the invention is that the method can be applied not [[just]] only in bus systems containing single-wire data lines but [[can]] also ~~be applied~~ in bus systems with two-wire data lines, since the electrical parameter determined is a differential voltage level at the output to the downstream control ~~appliance~~ device, as is obtained for determining signal transmission in line with the respective bus system on the data bus line.

[0031] The method can thus be used in a bus system based on the LIN (Local Interconnect Network) standard. In line with the LIN protocol, the data bus line provided is a single-wire data line for signal or data transmission. The signal transmission or evaluation takes place in the LIN bus by determining the differential voltage level between the LIN or the single-wire data line and the ground potential.

[0032] The method may likewise be used in a bus system with a two-wire data line, such as a CAN (Controller Area Network) data bus. For signal evaluation on a CAN bus, the voltage difference between the two data lines is measured, which is evaluated in the method as an electrical parameter.

[0033] One advantage of the invention is that in the case of a single-wire data line the electrical parameter measured is the current on the data line at the output to the downstream control ~~appliance~~ device, since current measurement is easy to implement in the control ~~appliance~~ device.

[0034] It has advantageously been recognized that if there is a downstream control ~~appliance~~ device which is to be addressed then the data line is closed again, using the isolating means[[,]] in the particular control ~~appliance in question~~ device which is to be addressed, and the transmission unit in [[the]] that particular control ~~appliance in question which is to be addressed is~~ device turned off. A control ~~appliance~~ device which is to be addressed thus forwards the address setting option to a further control ~~appliance~~ device which is to be addressed. ~~By means of~~ In this [[step,]] manner, it is possible to ascertain an individual control ~~appliance~~ device for address setting. [[The]] This step thus optimizes the method.

[0035] It is advantageous for the isolating means to be in the form of a switchable connection, such as a switching transistor or a relay or a repeater, which are available at low cost on the market today.

[0036] A further advantage of the method is that it may also be used in optical bus systems by ~~virtue of~~ using repeaters ~~being used~~ as the isolating means.

[0037] The fact that control ~~appliances~~ devices which are not involved in the addressing do not send any data to the data bus line in the address allocation period ~~of address allocation~~ prevents the address allocation from being disrupted.

In particular, this method allows the address allocation to be limited to the control ~~appliances~~ devices which are to be addressed which are involved.

[0038] It has advantageously been recognized that [[in]] during the address allocation period ~~of address allocation~~ no control ~~appliance~~ device is able to send a signal for connecting the control ~~appliances,~~ devices (that is, [[to say]] for closing the interrupted data line) [[,]] to all control ~~appliances~~ devices, since the data bus line is partially interrupted, of course. For this reason, the period of address allocation is limited to a time T_{MAX}. The control ~~appliances~~ devices involved in the address allocation restore the common data bus line by reconnecting the interrupted data bus line after the time T_{MAX}, which is known to every control ~~appliance~~ devices involved.

[0039] Advantageously, the start signal already contains the address which is to be allocated, which means that no further signal from a control ~~appliance~~ device is needed for the other control ~~appliances~~ device which are to be addressed.

[0040] It has advantageously been recognized that ~~the period of~~ address allocation period is produced as part of an addressing cycle and is started repeatedly by means of automatic flow control until an address setting has been made on all control ~~appliances~~ devices which are to be addressed.

[0041] The automatic flow control has the advantage that this needs to be performed only once using a control ~~appliance~~ device. After that, the control ~~appliances~~ devices automatically start the period of address allocation again

after a particular time T_{CYC}. In this context, T_{CYC} needs to be chosen to be greater than T_{MAX}, since ~~a period of~~ an address allocation period must [[needs]] to be concluded first, before a further period for renewed address allocation is started.

[0042] The automatic flow control may also be performed by virtue of a control ~~appliance~~ device repeatedly starting the ~~period for~~ address allocation period automatically, and accordingly transmitting an address which is to be allocated upon every start signal.

[0043] ~~The object is also achieved by a bus system in accordance with claim .... Accordingly~~ In one embodiment of the invention, the measuring arrangement has means for controlling the isolating means and the transmission/reception unit in the control ~~appliance~~ device in question, the means for control taking the evaluation of the measured signals as a basis for controlling the isolating means and the transmission/reception unit.

[0044] One advantage of this arrangement is that, by looping the data bus line through the control ~~appliance~~ device in conjunction with the isolating means contained in the control ~~appliance~~ device, the control ~~appliance~~ device is able to interrupt a common data bus line and also to reconnect it.

[0045] A further advantage is that the changes which are to be made can be implemented with minimal cost involvement on standard control ~~appliances~~ devices which are already in use on the market.

[0046] [[One]] Another advantage which has been recognized is that the development of the measuring arrangement has a comparison means which through simple comparison of input signals produces an output signal which is in turn used to control the transmission/reception unit and the isolating means.

[0047] Preferably, the comparison means is in the form of a comparator circuit on account of its switching speed.

~~There are now various options for advantageously refining and developing the disclosure of the present invention. In this regard, reference will first be made to the subordinate claims and secondly to the explanation of an embodiment which follows. The intention is also to include the advantageous refinements which are obtained from any combination of the subclaims. The drawings show an inventive apparatus for carrying out the inventive method. In these drawings, which are each a schematic illustration,~~

[0048] Other objects, advantages and novel features of the present invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings.

Brief Description of the Drawings

[0049] Figure 1 shows an inventive bus system for carrying out the inventive method; [[,]] and

[0050] Figure 2 shows a control ~~appliance~~ device with an inventive measuring arrangement.

Detailed Description of the Invention

[0051] The invention relates to a method for automatic address allocation by control ~~appliances~~ devices 3-6 connected to a bus system 1 in a ~~means of transport, where the~~ vehicle, such as shown in Figure 1. The control ~~appliances~~ devices 3-6 interchange data using transmission/reception units 10 via a common data bus line 2, ~~and the control appliances 3-6~~ simultaneously ~~access~~ accessing the data sent [[using]] via the ~~common~~ data bus ~~line 2~~. To this end, [[a]] an ~~period of~~ address allocation period is ~~started~~ initiated by [[means]] transmission of a message on the common data bus line 2. ~~After that, the~~ The message is taken as a basis, ~~in the period of address allocation,~~ for electrically breaking the common data bus line 2 into individual subsections during the address allocation period. ~~by virtue of~~ For this purpose, the control ~~appliances~~ devices 4-6 which are to be addressed ~~using a~~ use respective isolating means 9 ~~for the purpose of~~ to electrically break ~~breaking~~ the common data bus line 2. In addition, the control ~~appliances~~ devices 4-6 which are to be addressed place their respective transmission unit 10 at a transmission potential.

[0052] The ~~figure 1 has a~~ bus system 1 in Figure 1 is in the LIN standard (Local Interconnect Network – http://www.lin-subbus.org) with a data bus line and control ~~appliances~~ devices 3-6, the latter ~~control appliances 3-6~~ being engine control ~~appliances~~ devices for air conditioning applications in a motor ~~vehicles~~ vehicle. ~~The communication~~ Communication between the control ~~appliances~~ devices 3-6 takes place in [[line]] accordance with the LIN protocol, with equal authorization on the common data bus line.

[0053] ~~The data bus line is designed in line~~ In accordance with the LIN standard, ~~that is to say as a single wire line. The~~ the data bus line contains not only the actual single-wire ~~line, that is to say the actual~~ data or LIN line 2, but also a voltage supply line 8 and a line 7 which is connected to the ground potential. The differential voltage level U_{MEAS} measured on the data line 2 with respect to the ground line 7 is used to transmit and evaluate electrical signals ~~in line with~~ according to the LIN protocol. The data or messages sent on the data line 2 can be received by the control ~~appliances~~ devices 3-6 simultaneously.

[0054] The data line 2 is [[of]] bidirectional, and since ~~design. Since~~ the LIN standard is involved, ~~the data line 2~~ it is not terminated at the last subscriber in the bus system 1, control ~~appliance~~ device 6.

[0055] The data line 2 is rounted such that a [[for]] connection is provided between the subscribing control ~~appliances~~ devices 3-6 ~~is routed such that this connection is obtained by the control appliances 3-6~~. The data line is thus connected through between the input and output of the control ~~appliance~~ device.

[0056] ~~The control appliances 3-6 in figure 1 have, as~~ As transmission/reception unit 10, the control devices 3-6 in Figure 1 have an LIN transceiver or LIN bus driver, which ensures that the data are moved to the data line 2 in accordance with protocol. The transmission/reception unit (or the LIN transceiver) 10 is connected to the data line 2 within the control ~~appliance~~ device 3-6. In addition, the control ~~appliances~~ devices 3-6 have a voltage supply and a microcontroller (not shown) for performing their function-related tasks.

[0057] ~~For the time of~~ During the address allocation period, the control ~~appliance~~ device 3 undertakes the function of the master control ~~appliance~~ device and the control ~~appliances~~ devies 4-6 undertake the function of the slave control ~~appliances~~ devices.

[0058] The master control ~~appliance~~ device 3 has a programmed control algorithm which initiates, regulates and monitors [[the]] address allocation to the slave control ~~appliance~~ devices 4-6, ensuring ~~. The master control appliance 3 ensures~~ the correct address allocation ~~to the slave control appliances 4-6~~. The master control ~~appliance~~ device 3 thus knows the sequence or order and number of the slave control ~~appliances~~ device 4-6 which are connected to the bus system 1 and which are to be addressed.

[0059] [[The]] Each of the slave control ~~appliances~~ devices 4-6 have an isolating means 9 ~~which is~~ in the form of a switching transistor or switch ~~and which~~ that can be used to interrupt the data line 2. The switch 9 is positioned between the resistor 11 for the voltage supply line 8 [[,]] (the "pullup resistor") [[,]] and the LIN transceiver 10.

[0060] [[The]] Each of the control ~~appliances~~ devices 4-6 ~~each have~~ has a measuring arrangement (which has a comparator circuit as comparisong means) for determining the differential voltage level U_{MEAS}~~, which has a comparator circuit as comparison means~~. In addition, the measuring arrangement uses the control unit 17 (Figure 2) to control the switch 9 and the transmission/reception unit 10 based on the ~~basis of the~~ measurement result.

[0061] [[The]] Each of the slave control ~~appliances~~ devices 4-6 [[have]] has a programmed control algorithm which implements the method steps that ~~are to be executed by the slave control appliances 4-6~~ it is to extecute, particularly address setting, measurement of the differential voltage level U_{MEAS}, control of the switch 9 and of the LIN transceiver 10.

[0062] The voltage supply line 8 is connected to the data line 2 via a resistor 11, so that the LIN or data line 2 has a defined quiescent voltage, the "recessive level", of $U_{BAT} = 12$ V in the quiescent state. When the LIN transceiver 10 is turned on [[,]] (that is, [[to say]] a signal is sent), the data line 2 is connected through to the ground line 7, so that the differential voltage level U_{MEAS} falls to zero or ground potential, which corresponds to the "dominant level".

[0063] It should be noted that an LIN transceiver 10 behaves like a switch: upon turning it on [[,]] (that is, [[to say]] when a dominant level is sent), the data line 2 is connected to the ground line in order to obtain the zero signal "dominant level". Upon ~~interrupting it,~~ interruption (that is, [[to say]] when a recessive level is sent or in the quiescent state), the data line 2 is isolated from the ground line 7.

[0064] In the normal [[state]] operational mode, when the control ~~appliances~~ devices 3-6 communicate with equal authority [[using]] via the jointly used data line 2, the LIN transceivers 10 of the master and slave control ~~appliances~~ devices 3-6 which are involved are ready for transmission and reception. The switches 9 for breaking the data line 2 are closed and are thus connected through.

[0065] [[Upon]] The address allocation period is started by a message from the master control ~~appliance~~ device 3 on the common data line 2 to all connected control ~~appliances~~ devices 4-6~~, the period for address allocation is started~~. The message ~~from the master control appliance 3~~ already contains the address which is to be allocated. [[The]] Each of the slave control ~~appliances~~ devices 4-6 to be addressed immediately ~~use the~~ used its switch 9 to interrupt the data line 2. [[From]] (Accordingly, from this time onward, it is not possible to send data with equal authority to all control ~~appliances~~ devices 3-6 in the bus system, since the jointly used data line has been interrupted.) At the same time, the LIN transceiver 10 in the slave control ~~appliances~~ devices 4-6 which are to be addressed is turned on, so that a connection is made between the ground line 7 and the data line 2.

[0066] The control ~~appliances~~ devices 4-6 now monitor the differential voltage level U_{MEAS} at their respective output, with the differential voltage level U_{MEAS} [[being]] determined between the ground line 7 and the data line 2 to the downstream control ~~appliance~~ device 4-6. The differential voltage level U_{MEAS} is measured by the respective slave control ~~appliance~~ device 4-6 after a time T_{SG4}, T_{SG5}, T_{SG6} which is individually stipulated for each slave control ~~appliance~~ device 4-6 that is to be addressed and which has been disclosed to the respective control ~~appliance~~ device 4-6. Each slave control ~~appliance~~ device 4-6 takes the measurement result as a basis for deciding whether a further control ~~appliance~~ device to be addressed is connected downstream and decides, on the basis of the result, whether it remains a control ~~appliance~~ device to be addressed in this

address allocation period ~~of address allocation~~ or excludes itself from the address allocation in this address allocation period ~~of address allocation~~ by connecting the data line 2.

[0067] Since the differential voltage level U_{MEAS} is measured in every slave control ~~appliance~~ device 4-6 after its time, which is individually stipulated for [[the]] each control ~~appliance,~~ device (that is, [[to say]] for the control ~~appliance~~ device 4 after the time T_{SG4}, for the control ~~appliance~~ device 5 after the time T_{SG5} etc.), the recognition of whether there is a downstream control ~~appliance~~ device may also have been concluded for a control ~~appliance~~ device 4-6 at any position on the bus system 1 to start with.

[0068] It should be pointed out that the individual times T_{SG4}, T_{SG5}, T_{SG6} do not exceed a maximum value T_{MAX}. This maximum time period T_{MAX} is known to all control ~~appliances~~ devices 3-6 in the bus system 1, and is geared to the point from which the bus system 1 [[is]] becomes available for the joint data traffic again. At this time T_{MAX}, the data line isolating switch 9 in each of the control ~~appliances~~ devices 4-6 is closed.

[0069] If a control ~~appliance~~ device 4-6 to be addressed [[,]] (for example, [[a]] slave control ~~appliance~~ device 5) [[,]] has a further, downstream slave control ~~appliance~~ device 4-6 which is to be addressed in this address allocation period ~~of address allocation~~, (for example, control ~~appliance~~ device 6), available for it, then the voltage measurement produces the ground potential[[,]] (that is, [[to say]] a level which is dominant in line with the LIN protocol). The dominant level is obtained because the downstream slave control ~~appliance~~ device 6 which is to be

addressed has turned on its LIN transceiver 10, and the data line 2 is interrupted such that there is now only a connection between the "pullup resistor" 11 in the upstream control ~~appliance~~ device 5 and the turned-on LIN transceiver 11 in the downstream slave control ~~appliance~~ device 6.

[0070] [[If]] On the other hand, if a control ~~appliance~~ device 4-6 to be addressed[[,]] (for example, control ~~appliance~~ device 5) [[,]] does not have a downstream slave control ~~appliance~~ device 4-6 ~~, for example~~ (such as control ~~appliance~~ device 6), available, or if a slave control ~~appliance~~ device 4-6 which is not or no longer to be addressed in this period of address allocation period, then the result of the measurement U_{MEAS} is the supply voltage which is present on the data line 2 across the resistor 11[[,]] (that is, [[to say]] a level which is recessive in line with the LIN protocol). The recessive level is obtained because the downstream slave control ~~appliances~~ devices which are not involved in the addressing have connected the data line 2 running in the respective control ~~appliance~~ devices, and the respective LIN transceiver 10 is no longer turned on.

[0071] The measurement of the differential voltage level U_{MEAS} thus corresponds to a voltage measurement using a voltage divider. The voltage divider is formed by two resistors connected in series between the ground line 7 and the voltage supply line 8, where the "first resistor" corresponds to the pullup resistor 11 of a control ~~appliance~~ device and the "second resistor" corresponds to the LIN transceiver 10 of the downstream control ~~appliance~~ device. The measured voltage level at the voltage measurement point between the resistor 11

and the LIN transceiver 10 is determined by the switching of the LIN transceiver 10[[,]] (that is, [[to say]] open or closed).

[0072] If the measurement result [[means]] shows that the exemplary control ~~appliance~~ device 5 ~~contains~~ has a downstream control ~~appliance~~ device 6 which is to be addressed, then the LIN transceiver 10 in the control ~~appliance~~ device 5 is turned off and the data line 2 is connected by means of the switch 9. Hence, in this address allocation period, no address setting is performed on the control ~~appliance~~ device 5. It is necessary to wait for another address allocation period.

[0073] On the basis of their respective time T_{SG4}, T_{SG5}, T_{SG6}, the control ~~appliances~~ devices 4-6 to be addressed thus connect the data line 2 and turn off the LIN transceiver 10 until finally only the control ~~appliance~~ device 4 to be addressed which is connected last in the addressing cycle, as seen from the master control ~~appliance~~ device 3, now has its LIN transceiver 10 turned on and the data line 2 interrupted.

[0074] In the case of this control ~~appliance,~~ device (for example control ~~appliance~~ device 5), the data line 2 remains interrupted and the LIN transceiver 10 remains turned on until the time T_{MAX} has elapsed. Then, the address transmitted with the start message for the ~~period of~~ address allocation period is adopted. The addressing has been concluded for the control ~~appliance~~ device 5. The control ~~appliance~~ device 5 no longer involves itself in further addressing cycles under the prompting of the master control ~~appliance~~ device 3. In the address allocation period, the control ~~appliance~~ device 5 will no longer turn on its LIN transceiver 10, and ~~; the control appliance 5~~ does not send [[in]] during the

address allocation period. The data line 2 also remains connected in the control ~~appliance~~ device 5 for the ~~period of~~ address allocation period.

[0075] In further cycles, the remaining, as yet unaddressed control ~~appliances~~ devices, for example control ~~appliance~~ device 4, can now be addressed. [[Thus,]] That is, in a subsequent cycle, the slave control ~~appliance~~ device 4 now recognizes after the time T_{MAX} that there is no downstream slave control ~~appliance~~ device 5, 6 to be addressed, since the differential voltage measurement at the output of the slave control ~~appliance~~ device 4 does not produce a dominant level. The slave control ~~appliance~~ device 4 now adopts the address transmitted by the master control ~~appliance~~ device 3.

[0076] With this method, the address allocation is started beginning with the slave control ~~appliance~~ device 6 to be addressed which is connected last as seen from the master control ~~appliance~~ device 3. The last address allocation corresponds to the addressing of the slave control ~~appliance~~ device 4 to be addressed which is connected first as seen from the master control ~~appliance~~ device 3.

[0077] The order of the slave control ~~appliances~~ devices 4-6 in the connection arrangement on the bus system is crucial for the addressing. In each addressing cycle, it is always the control ~~appliance to be addressed~~ device which is connected last (as seen from the master control device) which is addressed, since this control ~~appliance~~ device cannot establish a downstream control ~~appliance~~ device which is to be addressed.

[0078] Figure 2 shows a measuring arrangement by way of example, as is implemented in the control ~~appliances~~ devices 4-6. The measuring arrangement has a comparator 13 with two inputs 14, 15 and an output 16. The output signal 16 from the comparator 13 is connected via a line to a control unit 17 which takes the comparator output signal as a basis for controlling the switch 9 and the transmission/reception unit 10 in the respective control ~~appliance~~ device 4; 5; 6. To this end, an input of the comparator 15 is placed at the potential of the data line 2 at the output of the control ~~appliance~~ device 4; 5; 6, which has a recessive or dominant voltage level. An input of the comparator 14 is placed constantly at the quiescent voltage of $U_{BATT} = 12$ V[[,]] (that is, [[to say]] at a recessive level which is tapped off between the ground line 7 and the voltage supply line 8 via resistors 12 in a voltage divider). From the comparison of the two input signals, the comparator ascertains an output signal which indicates whether the input signal 15 has a recessive or dominant voltage level. In line with this output signal, the control unit switches the switch 9 and the transmission/reception unit 10.

[0079] The master control ~~appliance~~ device 3 knows the order or the arrangement of the slave control ~~appliances~~ device 4-6 in relation to the master control ~~appliance~~ device 3. This means that the master control ~~appliance~~ device 3 is able to perform address allocation in line with the stipulations on the slave control ~~appliances~~ devices 4-6.

[0080] The method is not limited to bus systems based on the LIN protocol. Rather, it may likewise be used on bus systems such as CAN (Controller Area

Network), FlexRay, TTP (Time Triggered Protocol), D2B (Domestic Digital Bus), MOST (Media Oriented Systems Transport), since the latter's data communication is based on single-wire or two-wire data lines. In the case of bus systems with two-wire data lines, such as CAN, the switch 9 ~~needs to~~ must be present for both data lines.

[0081] The transmission/reception unit 10, in this case in the form of a LIN transceiver, is geared to the chosen bus protocol and bus system.

[0082] The switch 9 for switchably interrupting the data line 2 is in the form of a switching transistor. Alternatively, the switch may also be in the form of a relay. For bus systems whose data line 2 is ~~in the form of an~~ optical ~~data line~~, it is advantageous for the switch to be in the form of a repeater which does not forward the data during addressing, that is to say during interruption.

[0083] The exemplary embodiment is in the form of a "daisy chain" connection with series-connected control ~~appliances~~ devices 3-6, the master control ~~appliance~~ device 3 being positioned at one end of the series circuit, and the slave control ~~appliances~~ device 4-6 being connected downstream of the master control ~~appliance~~ device 3 in just one direction.

[0084] Alternatively, the method may be used in bus systems in which, for a series circuit, the slave control ~~appliances~~ devices 4-6 are situated to the left and right of the master control ~~appliance~~ device 3. In this case, the master control ~~appliance~~ device 3 simply behaves in the address allocation period like a control ~~appliance~~ device which is not to be addressed. The master control ~~appliance~~

device does not interrupt the data line and also does not turn on its transmission unit in the address allocation period. This means that bus systems with control ~~appliances~~ devices arranged in a series circuit require no isolating means[[,]] (that is, [[to say]] no additional modification) [[,]] for the master control ~~appliance~~ device.

[0085] In bus systems which are designed in a ring topology, the master control ~~appliance,~~ device (that is, [[to say]] the control ~~appliance~~ device which initiates the addressing) [[,]] has to interrupt the data bus line (and hence the ring) without switching in its transmission unit. The master control ~~appliance~~ device would thus need to have an isolating means for interrupting the data line, in the same manner as [[like]] the slave control ~~appliances~~ devices.

[0086] The measuring arrangement for measuring the electrical parameters may also be in the form of a current measuring device in a single-wire data line system like the LIN bus system. In this context, the measuring arrangement measures the current which flows from the output of the upstream slave control ~~appliance~~ device to the input of the downstream slave control ~~appliance~~ device.

[0087] The comparison means is in the form of a comparator circuit in the exemplary embodiment. Alternatively, the comparison may also be made by means of software[[,]] (that is, [[to say]] using a program). In this case, the comparison means is the processor with the software program running on it, which performs the comparison.

[0088] In addition, the control unit 17 and the comparison means 13 may be combined as one hardware chip, for example ASIC. This is suitable particularly when the comparison is performed by means of software.

[0089] In the exemplary embodiment, the address to be allocated is given at the same time as the start signal whenever the address allocation period starts. The address to be allocated can also be calculated by an algorithm implemented in the slave control ~~appliance~~ device, with the address to be allocated being formed automatically on an up-to-date basis using the algorithm. An example of such an algorithm is address counter imcrementation. ~~The address~~ Address allocation using an algorithm implemented in the slave control ~~appliance~~ is appropriate particularly in connection with automatic flow control of the addressing cycles. In this context, the master initiates the addressing only once. After that, the unaddressed slaves repeat this cycle after a common waiting time T_{CYC}, which ~~needs to~~ must be greater than T_{MAX}, the address allocation until the last slave control ~~appliance~~ device has been addressed.

[0090] The foregoing disclosure has been set forth merely to illustrate the invention and is not intended to be limiting. Since modifications of the disclosed embodiments incorporating the spirit and substance of the invention may occur to persons skilled in the art, the invention should be construed to include everything within the scope of the appended claims and equivalents thereof.